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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,326	06/26/2003	Shinji Yuri	Q75503	3189

7590 09/21/2005

SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037-3202

EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,326	YURI ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10,12-20 and 22* is/are pending in the application.

4a) Of the above claim(s) *7 and 13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-10,12,20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasebe et al., US Patent No. 6,744,135 in view of Toshiaki et al., Japanese Patent No. JP406152087A, and Urasaki et al., US Patent No. 5,689,879.

Regarding claim 1, Hasebe et al., in figure 7, discloses a multilayer wiring board, comprising: a metal substrate (metal substrate "M", as marked on figure 7 in appendix "A", shown as a metal plate 101 in more detail in figure 1(a), column 7, line 25-26) having first and second main surfaces (top and bottom surface as can be seen in figure 1(a)); a copper coating (copper coating "C", as marked on figure 7 in appendix "A", shown as copper plating 102 in more detail in figure 1(a), column 7, line 26-28) applied to at least one of the first and second main surfaces of the metal substrate and having a roughened surface (roughening the surface of copper plating, column 7, line 29-30); and an insulating resin layer (resin layers "R2", as marked on figure 7 in appendix "A", column 7, line 31-32) formed on the roughened surface of the copper coating. Though Hasebe et al., discloses the roughening of the surfaces for better adhesion, is silent about the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm.

Toshiaki et al., discloses (see abstract) copper layer in contact with insulation layer with a surface roughness (Ra) in the range of 1 to 1.6 μm, to achieve improved adhesion.

Urasaki et al., discloses a metal foil for printed wiring board with a first copper layer having a surface roughness suitable for adhering to a resin and capable of providing an electric circuit (column 3, line 40-44) and further discloses that the surface roughness of the first copper layer to be about 2 to 4 μm.

As recited by Toshiaki et al., and Urasaki et al., it is known in the art to have a surface roughness of a metal layer in the different ranges of 1 to 4 μm, and for that matter any suitable range for a better adhesion between the metal layer and the resin layer.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the wiring board of Hasebe et al., with an arithmetic mean roughness Ra of 0.1 to 10 μm, at taught by Toshiaki et al., and Urasaki et al., in order to have improved adhesion between the metal layer and the insulating resin layer.

Regarding claim 2, the modified wiring board of Hasebe et al., further discloses a wiring layer (wiring layer "W2", as marked on figure 7 in appendix "A") arranged on the insulating resin layer (resin layer "R2", as marked on figure 7 in appendix "A"); and a via (via "V1", as marked on figure 7 in appendix "A") extending through the insulating resin layer between the copper coating ("C") and the wiring layer ("W2").

Regarding claim 3, the modified wiring board of Hasebe et al., further discloses the copper coating has a thickness smaller than that of the metal substrate (thickness of 102 smaller than that of 101, as seen in figure 1(a)).

Regarding claim 4, the modified wiring board of Hasebe et al., further discloses the copper coating is copper plating (copper plating 102, see column 7, line 27-28).

Regarding claim 8, Hasebe et al., in figure 7, discloses a multilayer resin wiring board, comprising: a metal substrate (metal substrate "M", as marked on figure 7 in appendix "A", shown as a metal plate 101 in more detail in figure 1(a), column 7, line 25-26) having first and second main surfaces (top and bottom surface as can be seen in figure 1(a)) and defining therein a through hole (through hole "H", as marked on figure 7 in appendix "A", see column 13, line 42-42) extending between the first and second main surfaces; a copper coating (copper coating "C", as marked on figure 7 in appendix "A", shown in more detail as 304 in figure 3(b)) applied to the first and second main surfaces of the metal substrate and an inner surface of the through hole and having a

roughened surface (column 7, line 29-30); a plurality of insulating resin layers (resin layers "R1", "R2" , "R3" and "R4", as marked on figure 7 in appendix "A") and wiring layers (wiring layers "W1", "W2", "W3" and "W4" as marked on figure 7 in appendix "A") formed on the roughened surface of the copper coating to be located on the first and second main surfaces of the metal substrate, the insulating resin layers being interposed between the copper coating and the wiring layers or between the copper coating and the wiring layers and between the wiring layers (resin layers "R1", "R2" , "R3" and "R4", see marked up figure 7 in appendix "A"); a resin filler filled in the through hole (resin "RV" in the through hole "H", as marked on figure 7 in appendix "A"); a first via (via "V1", as marked on figure 7 in appendix "A") extending through the insulating resin layer between the copper coating and the wiring layer; and a second via (701) extending through the resin filler ("RV")and the insulating resin layers ("R1", "R2") between the wiring layer ("W1", "W2") located on the first main surface and the wiring layer located on the second main surface while being kept insulated from the metal substrate.

Though Hasebe et al., discloses the roughening of the surfaces for better adhesion, is silent about the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm.

Toshiaki et al., discloses (see abstract) copper layer in contact with insulation layer with a surface roughness (Ra) in the range of 1 to 1.6 μm, to achieve improved adhesion.

Urasaki et al., discloses a metal foil for printed wiring board with a first copper layer having a surface roughness suitable for adhering to a resin and capable of providing an electric circuit (column 3, line 40-44) and further discloses that the surface roughness of the first copper layer to be about 2 to 4 μm.

As recited by Toshiaki et al., and Urasaki et al., it is known in the art to have a surface roughness of a metal layer in the different ranges of 1 to 4 μm, and for that matter any suitable range for a better adhesion between the metal layer and the resin layer.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the wiring board of Hasebe et al., with an arithmetic mean roughness Ra of 0.1 to 10 μm, at taught by Toshiaki et al., and Urasaki et al., in order to have improved adhesion between the metal layer and the insulating resin layer.

Regarding claim 9, the modified wiring board of Hasebe et al., further discloses the copper coating has a thickness smaller than that of the metal substrate (thickness of 304 smaller than that of 301, as can be seen in figure 7 and 3(b)).

Regarding claim 10, the modified wiring board of Hasebe et al., further discloses copper coating is a copper plating (copper plating 102, column 7, line 27-28).

3. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the modified wiring board of Hasebe et al., (in combination with Toshiaki et al. and Urasaki et al.,) as applied to claims 1 and 8 above, and further in view of Masatoshi et al., (Japanese Patent No. JP401119620A), and Galasco et al., (US Patent No. 6,518,509).

Regarding claim 6, the applicant is further claiming the metal substrate is a rolled plate of metal or metal alloy having a thickness of 150 μm or larger.

The modified wiring board of Hasebe et al., discloses all the features of the claimed invention, as applied to claim 1 above and further recites the metal substrate is a metal alloy (42 alloy, iron-nickel alloy, column 7, line 25) having a thickness of larger than 150 μm (0.2 mm, 200 μm, which is larger than 150 μm, column 7, line 25-26). However, failed to explicitly recite the metal substrate is **a rolled plate**.

Masatoshi et al., discloses a metal substrate as a rolled plate (see abstract, rolling a Fe-Ni ingot into a plate to have desired thickness for superior magnetic properties and to reduce high frequency loss).

Galasco et al., discloses a metal substrate as a rolled plate (see back ground discussion, column 1, line 10-20, which recites that a copper invar copper (CIC) laminate of specified thickness and desired mechanical properties may be formed by rolling the feedstock of CIC sheet).

As recited by Masatoshi et al., and Galasco et al., it is conventional in the art to roll a plate to have the desired final thickness and is further known to use such plate as a metal substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe the metal plate of circuit board of Hasebe et al., as a rolled plate, as taught by Masatoshi et al., and Galasco et al., in order to have the metal substrate with desired thickness and mechanical/electrical properties.

Regarding claim 12, the applicant is further claiming the metal substrate is a rolled plate of metal or metal alloy having a thickness of 150 μm or larger.

Hasebe et al., discloses all the features of the claimed invention, as applied to claim 8 above and further recites the metal substrate is a metal alloy (42 alloy, iron-nickel alloy, column 7, line 25) having a thickness of larger than 150 μm (0.2 mm, 200 μm, which is larger than 150 μm, column 7, line 25-26). However, failed to explicitly recite the metal substrate is **a rolled plate**.

Masatoshi et al., discloses a metal substrate as a rolled plate (see abstract, rolling a Fe-Ni ingot into a plate to have desired thickness for superior magnetic properties and to reduce high frequency loss).

Galasco et al., discloses a metal substrate as a rolled plate (see back ground discussion, column 1, line 10-20, which recites that a copper invar copper (CIC) laminate of specified thickness and desired mechanical properties may be formed by rolling the feedstock of CIC sheet).

As recited by Masatoshi et al., and Galasco et al., it is conventional in the art to roll a plate to have the desired final thickness and is further known to use such plate as a metal substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe the metal plate of circuit board of Hasebe et al., as a rolled plate, as taught by Masatoshi et al., and Galasco et al., in order to have the metal substrate with desired thickness and mechanical/electrical properties.

4. Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Hasebe et al., US Patent No. 6,744,135, in view of Masatoshi et al., Japanese Patent No. JP401119620A, Galasco et al., US Patent No. 6,518,509, Siuzdak, US Patent No. 5,040,292, Toshiaki et al., Japanese Patent No. JP406152087A and Urasaki et al., US Patent No. 5,689,879.

Regarding claim 20, Hasebe et al., in figure 7, discloses a substrate material for a multilayer wiring board, comprising: a metal substrate (metal substrate "M", as marked on figure 7 in appendix "A", shown as 101 in more detail in figure 1(a), column 7, line 25-26) of Fe--Ni alloy (42 alloy, iron-nickel alloy, column 7, line 25) formed with a thickness of 150 μm or larger (0.2 mm, (=200 μm), which is larger than 150 μm, column 7, line 25-26)) and having first and second main surfaces (top and bottom surface as can be seen in figure 1(a)); and a copper coating (copper coating "C", as marked on figure 7 in appendix "A", shown as 102 in more detail in figure 1(a), column 7, line 26-

28) applied to at least one of the first and second main surfaces of the metal substrate, having a roughened surface (column 7, line 29-30).

Hasebe et al., does not disclose the metal plate being a rolled plate and copper coating being formed with a thickness of 5 μm or larger, and the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm.

Regarding the metal plate being rolled plate, Masatoshi et al., discloses a metal substrate as a rolled plate (see abstract, rolling a Fe-Ni ingot into a plate to have desired thickness for superior magnetic properties and to reduce high frequency loss).

Galasco et al., discloses a metal substrate as a rolled plate (see back ground discussion, column 1, line 10-20, which recites that a copper invar copper (CIC) laminate of specified thickness and desired mechanical properties may be formed by rolling the feedstock of CIC sheet).

As recited by Masatoshi et al., and Galasco et al., it is conventional in the art to roll a plate to have the desired final thickness and is further known to use such plate as a metal substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe the metal substrate of Hasebe et al., as a rolled plate of metal alloy, as taught by Masatoshi et al., and Galasco et al., in order to have the metal substrate with desired thickness and mechanical / electrical properties.

Regarding copper coating being formed with a thickness of 5 μm or larger, though Hasebe et al., is silent about the specific thickness of the copper coating, in the summary of invention recites the overall thermal conductivity of iron-nickel alloy metal plate can be improved by coating the metal plate by highly conductive copper coating (see in the summary of invention, page 3, column 3, line 34-40, Hasebe et al., recites that "in the case of using the high elastic metal having the iron-nickel as the main component mentioned above as the metal plate mentioned above, since they have a low coefficient of thermal conductivity, it is preferable that the structure is made such that a surface thereof is coated with a member having a high coefficient of thermal conductivity, for example, a copper plating (composite metal plate). This coating can be also effectively used at a time of executing a roughening process for improving an adhesion to an insulating resin".

This implies that the coefficient of thermal conductivity of the metal plate can be adjusted by providing a coating of high conductive material, such as copper, with a desired thickness to have the required thermal conductivity.

Siuzdak discloses a thermally conductive base (10) made of Invar, a nickel iron alloy, with thick copper coating layer (18) in the order of 1mil (25.4 μm), to have desired thermal conductive characteristics of the base (column 2, line 14-41).

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the metal substrate of Hasebe et al., with a copper coating formed with a thickness of 5 μm or larger, as taught by Siuzdak, in order to have desired thermal conductive characteristics of the metal substrate.

Regarding the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm, Toshiaki et al., discloses (see abstract) copper layer in contact with insulation layer with a surface roughness (Ra) in the range of 1 to 1.6 μm, to achieve improved adhesion.

Urasaki et al., discloses a metal foil for printed wiring board with a first copper layer having a surface roughness suitable for adhering to a resin and capable of providing an electric circuit (column 3, line 40-44) and further discloses that the surface roughness of the first copper layer to be about 2 to 4 μm.

As recited by Toshiaki et al., and Urasaki et al., it is known in the art to have a surface roughness of a metal layer in the different ranges of 1 to 4 μm, and for that matter any suitable range for a better adhesion between the metal layer and the resin layer.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the wiring board of Hasebe et al., with an

arithmetic mean roughness Ra of 0.1 to 10 μm, at taught by Toshiaki et al., and Urasaki et al., in order to have improved adhesion between the metal layer and the insulating resin layer.

5. Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hasebe et al., US Patent No. 6,744,135, in view of Masatoshi et al., Japanese Patent No. JP401119620A, Galasco et al., US Patent No. 6,518,509, Toshiaki et al., Japanese Patent No. JP406152087A and Urasaki et al., US Patent No. 5,689,879.

Regarding claim 22, Hasebe et al., in figure 7, discloses a substrate material for a multilayer wiring board, comprising: a metal substrate (metal substrate "M", as marked on figure 7 in appendix "A", shown as 101 in more detail in figure 1(a), column 7, line 25-26) of Fe--Ni alloy (42 alloy, iron-nickel alloy, column 7, line 25) formed with a thickness larger than 150 μm (0.2 mm, (=200 μm), which is larger than 150 μm, column 7, line 25-26)), having first and second main surfaces and defining therein a through hole (a hole out side via 701, shown in more detail at 309, figure 3(d)) extending between the first and second main surfaces; and a copper coating (copper coating "C", as marked on figure 7 in appendix "A", shown in more detail as 304 in figure 3(b)) applied to the first and second main surfaces of the metal substrate and an inner surface of the through hole and having a roughened surface (column 7, line 29-30).

Hasebe et al., does not disclose the metal plate being **a rolled plate** and the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm.

Regarding the metal plate being a rolled plate, Masatoshi et al., discloses a metal substrate as a rolled plate (see abstract, rolling a Fe-Ni ingot into a plate to have desired thickness for superior magnetic properties and to reduce high frequency loss).

Galasco et al., discloses a metal substrate as a rolled plate (see back ground discussion, column 1, line 10-20, which recites that a copper invar copper (CIC) laminate of specified thickness and desired mechanical properties may be formed by rolling the feedstock of CIC sheet).

As recited by Masatoshi et al., and Galasco et al., it is conventional in the art to roll a plate to have the desired final thickness and is further known to use such plate as a metal substrate.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe the metal substrate of Hasebe et al., is a rolled plate of metal alloy, as taught by Masatoshi et al., and Galasco et al., in order to have the substrate with desired thickness and mechanical / electrical properties.

Regarding the roughened surface has an arithmetic mean roughness Ra of 0.1 to 10 μm, Toshiaki et al., discloses (see abstract) copper layer in contact with insulation layer with a surface roughness (Ra) in the range of 1 to 1.6 μm, to achieve improved adhesion.

Urasaki et al., discloses a metal foil for printed wiring board with a first copper layer having a surface roughness suitable for adhering to a resin and capable of providing an electric circuit (column 3, line 40-44) and further discloses that the surface roughness of the first copper layer to be about 2 to 4 μm.

As recited by Toshiaki et al., and Urasaki et al., it is known in the art to have a surface roughness of a metal layer in the different ranges of 1 to 4 μm, and for that matter any suitable range for a better adhesion between the metal layer and the resin layer.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the wiring board of Hasebe et al., with an arithmetic mean roughness Ra of 0.1 to 10 μm, at taught by Toshiaki et al., and Urasaki et al., in order to have improved adhesion between the metal layer and the insulating resin layer.

Response to Arguments

6. Applicant's arguments filed on June 28, 2005 have been fully considered but they are not persuasive. Applicant argues that Hasebe does not specifically mention the roughening process copper coating and fails to disclose or teach at least Applicant's claimed arithmetic mean roughness range for the surface of copper coating. Applicant further argues that though the secondary art of Toshiaki et al., and Urasaki discloses the surface roughness, the they are structurally different from the wiring board of the

present invention and states that a person skilled in the art would not have been motivated to combine Hasebe et al., with Toshiaki et al., and Urasaki.

This is not found persuasive. The examiner recognizes that the references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references, however there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. The primary art of Hasebe et al., discloses the roughened surface for better adhesion but does not disclose specific range of the roughness. The secondary art of Toshiaki et al., and Urasaki are used to further support that various roughness, including that claimed in the instant claims, are known in the art to have desired adhesion. It would have been obvious to a person of ordinary skill in the art to have roughness in the desired range to have better adhesion. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mitsuhashi et al., US Patent No. 6,475,638 discloses electrodeposited copper foil with surface roughness (Rz) from about 0.8 to 2.5 μm on one side and 2.5 to 10 μm on the other side (column 15, line 19-35).

Kuwako et al., US Patent No. 6,693,793, discloses electrically conductive layers with roughening for bond enhancement and state that it can be done by micro-etching, by electrolytically treating to form a roughened copper deposit, or by electrolytically treating with a deposition of micro-nodules (column 5, line 35-45).

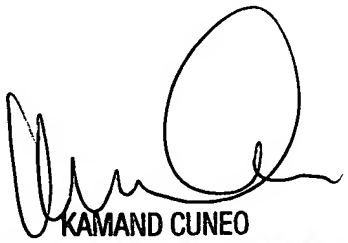
8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
September 16, 2005